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EXAMINER	
YIGDALL, MICHAEL J	

ART UNIT	PAPER NUMBER
2192	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/802,857	KOH ET AL.	
	Examiner	Art Unit	
	Michael J. Yigdall	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 September 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *53-69* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *53-69* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office action is responsive to Applicant's reply filed on September 23, 2010. Claims 53-69 are now pending.

Response to Arguments

2. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection set forth below. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action.

Claim Rejections under 35 U.S.C. § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. § 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 63 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter that Applicant regards as the invention.

With respect to claim 63 (new), there is insufficient antecedent basis in the claims for "said first bug address" and "said second bug address" such as recited in the claim. The examiner presumes that Applicant intended the claim to recite "a first bug address" and "a second bug address" instead.

Claim Rejections under 35 U.S.C. § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 53, 55-59 and 64-69 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,784,537 to Suzuki et al. (already of record, "Suzuki").

With respect to claim 53 (new), Suzuki teaches a data processing apparatus comprising:

a central processing unit (see, for example, CPU 14 in FIG. 1) configured to initiate execution of an interrupt processing routine upon a transition of an interrupt request signal (see, for example, step S11 in FIG. 4B and column 6, lines 27-36, which shows that the CPU 14 is configured to execute interrupt processing upon transition of an interrupt request signal), a first signal and a second signal being input to said central processing unit as said interrupt request signal (see, for example, step S5 in FIG. 4A, steps S28, S29 and S30 in FIG. 4B, and column 6, line 65 to column 7, line 2, which shows that S number of interrupt request signals are input to the CPU 14).

With respect to claim 55 (new), the rejection of claim 53 is incorporated, and Suzuki further teaches that said first and second signals are input to said central processing unit as a single signal (see, for example, FIG. 4B, which shows that the S number of signals are input to the CPU 14 as a single signal S number of times).

With respect to claim 56 (new), the rejection of claim 53 is incorporated, and Suzuki further teaches that said first and second signals are input to said central processing unit as two

different signals (see, for example, FIG. 4B, which shows that the S number of signals are input to the CPU 14 as S number of different signals).

With respect to claim 57 (new), the rejection of claim 53 is incorporated, and Suzuki further teaches that said central processing unit executes a program code, said program code being stored in memory at a program address (see, for example, column 3, lines 64-67, which shows that the CPU 14 executes program code stored in ROM 18, inherently at a program address).

With respect to claim 58 (new), the rejection of 57 is incorporated, and Suzuki further teaches that said program address is a count of a program counter (see, for example, column 4, lines 12-16, which shows that the program address is a program counter value).

With respect to claim 59 (new), the rejection of claim 57 is incorporated, and Suzuki further teaches that said memory is read only memory (see, for example, column 3, lines 64-67, which shows that the memory is ROM 18).

With respect to claim 64 (new), the rejection of claim 57 is incorporated, and Suzuki further teaches that said first signal indicates when said program address and a first bug address coincide, said second signal indicating when said program address and a second bug address coincide (see, for example, column 6, lines 27-36, which shows that each of the S number of signals indicates that the program address and a correction address coincide).

With respect to claim 65 (new), the rejection of claim 64 is incorporated, and Suzuki further teaches that a first coincidence detecting circuit compares said program address with said

first bug address, said first coincidence detecting circuit outputting said first signal when said program address and said first bug address coincide (see, for example, ROM correction processing circuit 24 in FIG. 1 and column 4, lines 12-26, which shows that the circuit compares the program address with the correction address and outputs the signal when the program address and the correction address coincide).

With respect to claim 66 (new), the rejection of claim 65 is incorporated, and Suzuki further teaches a second coincidence detecting circuit compares said program address with said second bug address, said second coincidence detecting circuit outputting said second signal when said program address and said second bug address coincide (see, for example, ROM correction processing circuit 24 in FIG. 1 and column 4, lines 12-26, which shows that the circuit compares the program address with the correction address and outputs the signal when the program address and the correction address coincide).

With respect to claim 67 (new), the rejection of claim 66 is incorporated, and Suzuki further teaches that a number of times said first and second bug addresses coincide with said program address is counted, a value representing said number of times (see, for example, FIG. 2B and column 4, lines 41-49, which shows a value in the two most significant bits of a register that represents a number of parts of a program to be corrected, or the number of correction addresses, and see, for example, step S5 in FIG. 4A and step S28 in FIG. 4B, which shows storing the value and counting down the stored value each time the program address coincides with a correction address, such that the value of the count subtracted from S represents the number of times the addresses coincide).

With respect to claim 68 (new), the rejection of claim 67 is incorporated, and Suzuki further teaches or suggests that said first bug address indicates a starting address for a first buggy part of a program or data, said second bug address indicating a starting address for a second buggy part of said program or data (see, for example, column 5, lines 10-14, which shows that each correction address indicates a starting address for a part of a program to be corrected).

With respect to claim 69 (new), the rejection of claim 68 is incorporated, and Suzuki further teaches or suggests that said first buggy part or said second buggy part is selected for correction, said central processing unit using said value to select said first buggy part or said second buggy part (see, for example, column 6, line 65 to column 7, line 7, which shows that the part of the program to be corrected is selected for correction based on the value).

7. Claims 53-57 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,875,342 to Temple (now made of record, "Temple").

With respect to claim 53 (new), Temple teaches a data processing apparatus comprising:

a central processing unit (see, for example, CPU 101 in FIG. 1) configured to initiate execution of an interrupt processing routine upon a transition of an interrupt request signal (see, for example, column 6, lines 8-12, which shows that the CPU 101 is configured to process an interrupt upon transition of an interrupt request signal), a first signal and a second signal being input to said central processing unit as said interrupt request signal (see, for example, column 5, lines 42-47, which shows that a plurality of interrupt request signals are input to the CPU 101).

With respect to claim 54 (new), the rejection of claim 53 is incorporated, and Temple further teaches that said first and second signals are input to an AND gate, an output from said AND gate being input to said central processing unit as said interrupt request signal (see, for example, AND gates 203 and 205 in FIG. 2, which shows that the plurality of signals are input to an AND gate and that an output from the AND gate is input to the CPU 101 as the interrupt request signal).

With respect to claim 55 (new), the rejection of claim 53 is incorporated, and Temple further teaches that said first and second signals are input to said central processing unit as a single signal (see, for example, FIG. 2, which shows that the plurality of signals are input to the CPU 101 as a single signal).

With respect to claim 56 (new), the rejection of claim 53 is incorporated, and Temple further teaches that said first and second signals are input to said central processing unit as two different signals (see, for example, column 5, lines 42-47, which shows that the plurality of signals are input to the CPU 101 as a plurality of different signals at different priority levels).

With respect to claim 57 (new), the rejection of claim 53 is incorporated, and Temple further teaches that said central processing unit executes a program code, said program code being stored in memory at a program address (see, for example, storage unit 102 in FIG. 1 and column 9, lines 44-48, which shows that the CPU 101 executes program code stored in memory, inherently at a program address).

Claim Rejections under 35 U.S.C. § 103

8. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 54 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Suzuki, as applied to claim 53 above, in view of Temple.

With respect to claim 54 (new), the rejection of claim 53 is incorporated. Suzuki does not explicitly describe that said first and second signals are input to an AND gate, an output from said AND gate being input to said central processing unit as said interrupt request signal.

However, in an analogous art, Temple teaches a central processing unit (see, for example, CPU 101 in FIG. 1) configured to initiate execution of an interrupt processing routine upon a transition of an interrupt request signal (see, for example, column 6, lines 8-12, which shows that the CPU 101 is configured to process an interrupt upon transition of an interrupt request signal), a first signal and a second signal being input to said central processing unit as said interrupt request signal (see, for example, column 5, lines 42-47, which shows that a plurality of interrupt request signals are input to the CPU 101). Temple further teaches that said first and second signals are input to an AND gate, an output from said AND gate being input to said central processing unit as said interrupt request signal (see, for example, AND gates 203 and 205 in FIG. 2, which shows that the plurality of signals are input to an AND gate and that an output from the

AND gate is input to the CPU 101 as the interrupt request signal). The teachings of Temple provide an interrupt controller for processing a plurality of interrupts at different priority levels (see, for example, column 5, lines 42-47).

Therefore, as Temple suggests, it would have been obvious to those of ordinary skill in the art at the time the invention was made to implement the data processing apparatus of Suzuki such that said first and second signals are input to an AND gate, an output from said AND gate being input to said central processing unit as said interrupt request signal.

10. Claims 54 and 60-63 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Suzuki, as applied to claims 53 and 57 above, respectively, in view of U.S. Patent No. 5,357,627 to Miyazawa et al. (already of record, "Miyazawa").

With respect to claim 54 (new), the rejection of claim 53 is incorporated. Suzuki does not explicitly describe that said first and second signals are input to an AND gate, an output from said AND gate being input to said central processing unit as said interrupt request signal.

However, in an analogous art, Miyazawa teaches a plurality of program correction units, 3C-1 to 3C-m, each outputting a signal when a program address and a bug address coincide (see, for example, FIG. 12 and column 9, lines 39-58). The plurality of signals are input to an OR gate 40, and an output from the OR gate 40 is provided as an interrupt request signal (see, for example, FIG. 12 and column 9, line 59 to column 10, line 5, and column 10, lines 32-41). The teachings of Miyazawa provide for correcting a plurality of bugs in the program (see, for example, column 2, lines 9-25).

In Miyazawa, the program correction circuit 3C is implicitly defined as "active high." If the program correction circuit 3C is instead defined as "active low," a person of ordinary skill in the art could, with predictable results, substitute the OR gate 40 with an AND gate to provide the same results. The truth tables below illustrate:

Active high (a "1" level represents a coincidence between the addresses)

First signal (S_1)	Second signal (S_2)	S_1 OR S_2	Result
0	0	0	No Interrupt
0	1	1	Interrupt
1	0	1	Interrupt
1	1	1	Interrupt

Active low (a "0" level represents a coincidence between the addresses)

First signal (S_1)	Second signal (S_2)	S_1 AND S_2	Result
1	1	1	No Interrupt
1	0	0	Interrupt
0	1	0	Interrupt
0	0	0	Interrupt

Therefore, as Miyazawa suggests, it would have been obvious to those of ordinary skill in the art at the time the invention was made to implement the data processing apparatus of Suzuki such that said first and second signals are input to an AND gate, an output from said AND gate being input to said central processing unit as said interrupt request signal.

With respect to claim 60 (new), the rejection of claim 57 is incorporated. To the extent Suzuki does not explicitly describe that said memory is random access memory, such an implementation nonetheless would have been obvious to those of ordinary skill in the art.

For example, Suzuki teaches a random access memory for storing data when the program code is executed (see, for example, RAM 16 in FIG. 1 and column 4, lines 1-5). Moreover, in an analogous art, Miyazawa teaches a correction program RAM 74 that stores correction program data (see, for example, FIG. 14 and column 11, lines 7-13).

A person of ordinary skill in the art could, with predictable results, implement the data processing apparatus of Suzuki such that said memory is a random access memory. Therefore, as Suzuki and Miyazawa suggest, the claimed subject matter would have been obvious to those of ordinary skill in the art at the time the invention was made.

With respect to claim 61 (new), the rejection of claim 60 is incorporated, and Suzuki in view of Miyazawa further teaches or suggests that said interrupt processing routine is stored in said random access memory (see, for example, Miyazawa, FIG. 13 and column 10, lines 6-24, which shows a subroutine for interrupt processing stored in a PROM 31, and column 3, lines 39-48, which shows that the PROM represents a random access memory).

With respect to claim 62 (new), the rejection of claim 60 is incorporated, and Suzuki in view of Miyazawa further teaches or suggests that an abort vector is stored in said random access memory, said abort vector designating a start address of said interrupt processing routine (see, for example, Miyazawa, column 9, line 39 to column 10, line 5, which shows a vector address area 34 in a PROM 31 that stores a start address for interrupt processing, and column 3, lines 39-48, which shows that the PROM represents a random access memory).

With respect to 63 (new), the rejection of claim 60 is incorporated. To the extent Suzuki in view of Miyazawa does not explicitly describe that a counter register is located within said

random access memory, said counter register being incremented when said program address coincides with said first bug address or said second bug address, such an implementation nonetheless would have been obvious to those of ordinary skill in the art.

For example, Suzuki teaches a value in the two most significant bits of a register that represents a number of parts of a program to be corrected, or a number of correction addresses (see, for example, Suzuki, FIG. 2B and column 4, lines 41-49), and further teaches that such values are stored in the RAM 16 when the program code is executed (see, for example, column 4, lines 1-5). Moreover, Suzuki teaches storing a value that represents the number of correction addresses and counting down the stored value each time the program address coincides with a correction address, such that the value of the count subtracted from S represents the number of times the addresses coincide (see, for example, step S5 in FIG. 4A and step S28 in FIG. 4B).

In Suzuki, the count (i.e., the counter register) is decremented when the program address coincides with a correction address. However, a person of ordinary skill in the art could, with predictable results, implement the data processing apparatus of Suzuki such that the counter register is incremented rather than decremented. Specifically, with reference to FIGS. 4A and 4B, given the number of correction addresses S, a person of ordinary skill in the art could initialize the value to 0 (rather than S) in step S5, increment (rather than decrement) the stored value in step S28, and check whether the stored value is equal to S (rather than 0) in step S29. Such an implementation is analogous to the one described in Suzuki and provides the intended results. Indeed, as evidenced in the Suzuki reference, incrementing the value of a counter register is within the level of ordinary skill in the art (see, for example, step S88 in FIG. 12B and

column 9, lines 52-54). In such an implementation, the stored value (i.e., the value of the counter register) would represent the number of times the addresses coincide.

Therefore, as Suzuki suggests, it would have been obvious to those of ordinary skill in the art at the time the invention was made to implement the data processing apparatus of Suzuki such that a counter register is located within said random access memory, said counter register being incremented when said program address coincides with said first bug address or said second bug address.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure (see the attached Notice of References Cited).

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Yigdall whose telephone number is (571) 272-3707. The examiner can normally be reached on Monday to Friday from 9:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Michael J. Yigdall/
Primary Examiner, Art Unit 2192